ELECTRICAL IMPACT CHARACTERIZATION OF ANODE ACTIVE AREA AND STACKING-FAULTS IN 6.5 KV 4H-SIC PIN DIODES

NGHIÊN CỨU ẢNH HƯỞNG CỦA DIỆN TÍCH BỀ MẶT DẪN ĐIỆN VÀ CÁC LỖI XẾP CHỒNG ĐẾN ĐẶC TÍNH CỦA ĐIỐT PiN 4H-SIC

Nguyen Duy Minh[1,*], Nguyen Manh Quan[2]

ABSTRACT

This paper reports on the design and characterization of 6.5kV class 4H-SiC PiN diodes with different active areas of 2, 8, and 24mm^2. Diodes edge termination is a combination of MESA and JTE. The blocking voltage of 6.5kV was achieved on the three types of diodes. Diodes operation stability is studied in term of temperature dependence and DC stress. In the limit of used package, these diodes present a stable operation until 225°C. The reverse leakage current at 225°C is less than 3µA at 3kV for 24mm^2 diodes. The forward voltage drop decreases with the increasing temperature but the voltage change is low, less than 0.5V in the temperature range of (25°C - 225°C). After a DC stress under current density as high as 100A.cm^{-2}, an important on-state forward voltage drift has been observed. This voltage drift is explained by the generation and prolongation of stacking-faults (SFs) which result in the reduction of carrier lifetime. A reduction of up to two times has been measured by open-circuit voltage decay (OCVD) technique. These diodes are also characterized by mean of admittance spectroscopy vs. temperature. These measures revealed an electronic energy level at 0.18eV under the conduction band for the stressed diodes thus this energy level can be attributed to an electrical signature of SFs.

Keywords: *4H-SiC, PiN diode, MESA, JTE, Stacking-faults, OCVD.*

TÓM TẮT

Bài báo trình bày thiết kế, kết quả thử nghiệm và phân tích điốt công suất PiN điện áp 6,5kV chế tạo trên nền vật liệu SiC với các kích thước bề mặt dẫn dòng 2, 8 và 24mm^2. Các điốt được thiết kế bảo vệ bằng sự kết hợp cấu trúc MESA và JTE. Điện áp cực đại đạt được 6,5kV trên cả ba kích thước điốt. Sự hoạt động ổn định của điốt được nghiên cứu trong các điều kiện nhiệt độ khác nhau và với mật độ dòng điện lớn. Trong giới hạn của cấu trúc dùng để đóng gói điốt (lớp vỏ), các điốt được thử nghiệm hoạt động ổn định đến nhiệt độ 225^{0}C. Dòng điện rò ở nhiệt độ 225^{0}C đo được nhỏ hơn 3µA ở điện áp phân cực ngược 3kV đối với điốt cỡ 24mm^2. Sụt áp khi phân cực thuận bị giảm khi nhiệt độ tăng tuy nhiên sự thay đổi này là rất bé, nhỏ hơn 0,5V trong khoảng nhiệt độ thử nghiệm (25°C - 225°C). Sau khi điốt chịu áp lực dẫn dòng liên tục ở mật độ dòng điện cao 100A.cm^{-2}, điện áp phân cực thuận đo được trên điốt bị trôi một khoảng khá lớn. Sự gia tăng điện áp phân cực thuận này có thể giải thích bởi sự hình thành và phát triển của các lỗi xếp chồng trong cấu trúc bán dẫn của điốt dẫn đến sự suy giảm thời gian sống của các hạt mang điện. Sự suy giảm thời gian sống lên đến 2 lần đã đo được bằng kỹ thuật đo độ giảm điện áp khi hở mạch. Phương pháp đo phổ điện dẫn theo nhiệt độ cũng được áp dụng với các điốt này phát hiện ra một mức năng lượng 0,18eV nằm dưới dải dẫn đối với các điốt chịu áp lực dòng liên tục lớn. Mức năng lượng này không xuất hiện ở các điốt trước khi chịu áp lực dòng do đó có thể nói mức năng lượng này là một đặc trưng điện của sự xuất hiện các lỗi xếp chồng trong cấu trúc điốt.

Từ khóa: *4H-SiC, điốt PiN, MESA, JTE, lỗi xếp chồng, OCVD.*

[1]Faculty of Electrical Engineering, Electric Power University
[2]Faculty of Electrical Engineering, Hanoi University of Industry
[*]Email: minhnd81@epu.edu.vn
Received: 25 October 2019
Revised: 15 January 2020
Accepted: 20 February 2020

1. INTRODUCTION

4H silicon carbide (4H-SiC) is a wide band gap semiconductor. Its excellent physical properties respond to increasing demand of modern power electronic applications. Indeed, sectors such as transport, electricity distribution and oil exploitation require devices operating at higher temperature and/or higher voltage [1]. The following works take part in the thematic of high voltage and high temperature devices in SiC. Nowadays, high voltage devices in Si are limited in term of junction operating temperature at 125°C. One potential of SiC bipolar diodes is to work at higher junction temperature thus to reduce the cooling system size. The first section of this paper describes the diodes design leading to the masks fabrication. After a brief description of technological process, diodes characterization will be presented for both forward and reverse modes and in function of temperature. The diodes have also been stressed at high forward current density in DC mode. Electrical characteristics evolution is detailed and physical interpretations of this evolution are also presented and discussed.

2. DIODES DESIGN AND FABRICATION

The schematic structure of developed diodes is presented in

Fig. 1. For a blocking voltage of 6.5kV, the devices have a vertical structure. Diodes edge termination is defined by a combination of MESA (etching of SiC) and JTE (Junction Termination Extension).

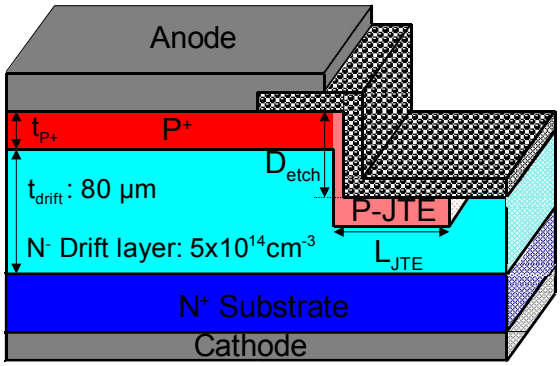


Figure 1. Schematic cross-section of the 6.5kV 4H-SiC bipolar diodes

Simulations by finite elements method using Sentaurus™ TCAD software [2] have been performed to determine the parameters of the drift region such as thickness (W_{N-}) and doping (N_D). The objective of these simulations is also to estimate the blocking voltage in function of different structure parameters such as etching depth (D_{etch}), JTE length (L_{JTE}), and JTE dose (P-JTE).

First, the parameters of the drift region have been determined by simulating the diode performance in forward and reverse mode. A compromise between the blocking voltage and the on-state forward voltage drop must be specified. The chosen parameters are: W_{N-}= 80µm and N_D= 5×10^{14}cm^{-3} for a theoretical blocking voltage of 11800V with the ionization coefficients reported in [3]. A safety margin in blocking voltage has been taken to include the incertitudes with respect to SiC technology that is not yet quite mature.

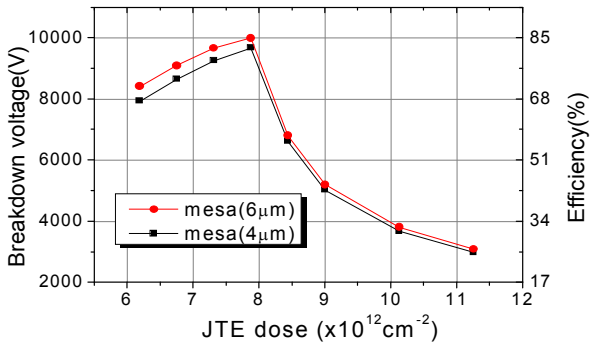


Figure 2. Diode blocking voltage and efficiency percentage evolution in function of active JTE dose for two different etching depths

Fig. 2 shows the blocking voltage evolution in function of active JTE dose for two different etching depths of a diode with the drift region parameters presented above. The JTE length is fixed at 400µm since we have not observed the effect of a longer JTE. With this kind of edge termination, the maximum efficiency is about 85%. The increase of etching depth has a slight influence on the blocking voltage when the JTE dose is lower than the optimum value. In this latter case, the breakdown takes place at the limit of the main junction and the JTE. Thus the slight increase of blocking voltage is probably due to the additional influence of MESA relative to JTE dose. By contrast, when the JTE is too doped, the breakdown takes place at the end of JTE so the etching depth has no influence on the blocking voltage. The different parameters (D_{etch}, L_{JTE}, P-JTE) have been optimized to obtain the maximum blocking voltage. Chosen values for D_{etch}, L_{JTE}, and P-JTE are respectively 6µm, 400µm, and 8×10^{12}cm^{-2}. Then, diodes masks have been designed with different active areas (2, 8 and 24mm^2) and diodes fabrication has been realized. Our objective is to examine the impact of active area on the blocking voltage.

3. DIODES CHARACTERIZATION

3.1. Reverse characteristics

Diodes wafer-level measurements have been performed on a semi-automatic probe station in a high vacuum chamber, this equipment allows to measure high voltage devices up to 20kV. As seen in Fig. 3, the blocking voltage of 6.5kV has been achieved on the three active area diodes.

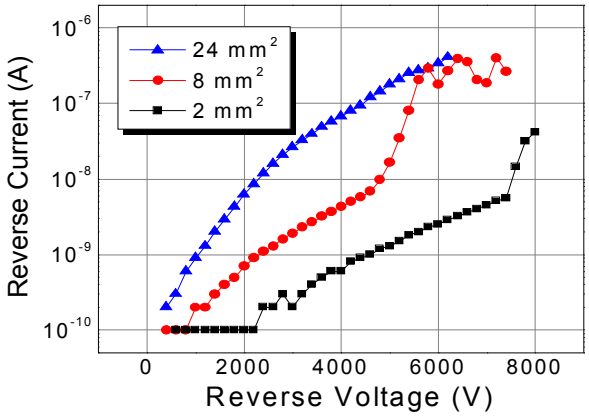
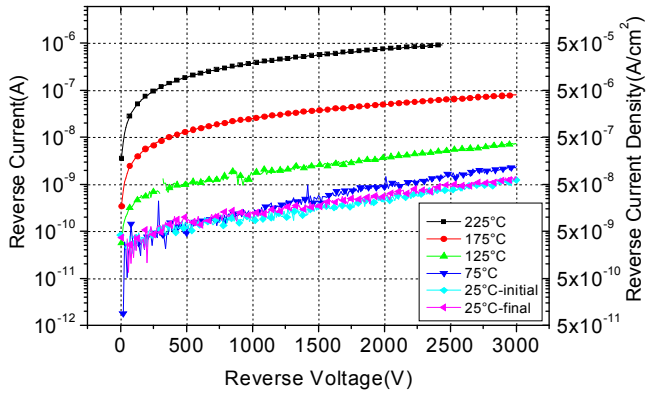
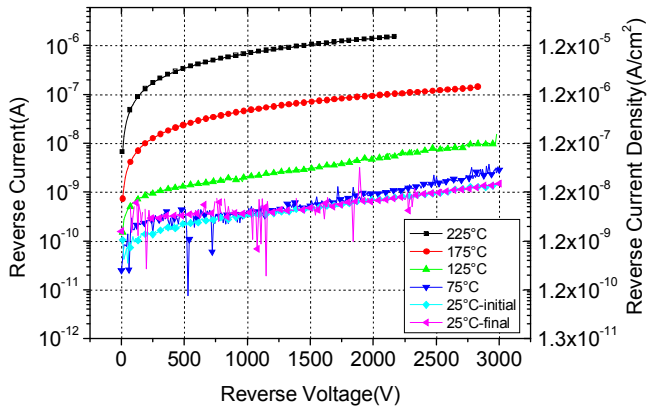


Figure 3. Reverse characteristics of the best fabricated 6.5kV diodes for three different areas

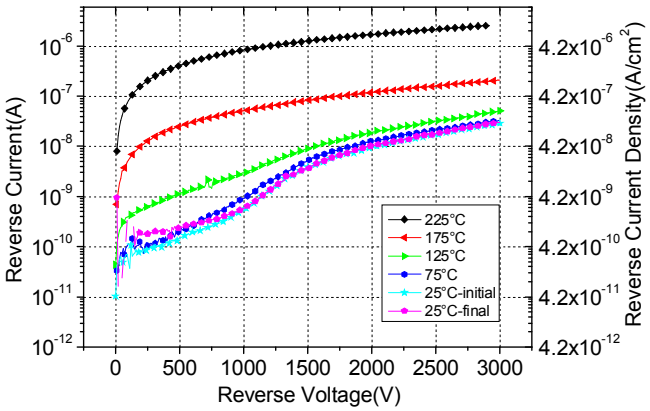
After wafer dicing, diode has been encapsulated in a TO3 type case. Temperature dependence of reverse characteristics has been measured up to 3kV. Temperature range is between 25°C and 225°C. The upper temperature limit is the limit of the gel used for the diodes encapsulation. Typical reverse characteristics are presented respectively in Fig. 4 (a, b, c) for 2, 8, and 24mm^2 diode. A pulse-air system is used to control the temperature. Characterizations have been performed up to 3kV because of equipment limitations. The leakage current increases with temperature but it is still as low as less than 5µA at 225°C. At 3kV and in the temperature range, the leakage current evolutes from 30nA to 3µA for the 24mm^2 diode and from 3nA to 2µA for the 2 and 8mm^2 diode. This increase is due to the density increase of carrier generation centers with temperature. This evolution is reversible because the difference of characteristics before and after stress is not significative.



(4a)



(4b)



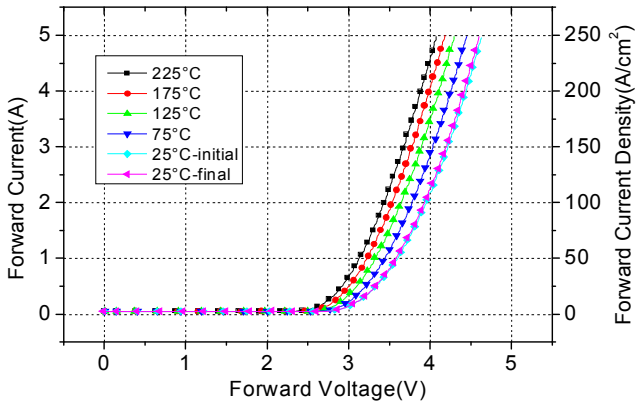
(4c)

Figure 4. Reverse characteristics temperature dependence of 2mm² (4a), 8mm² (4b) and 24mm² (4c) diode

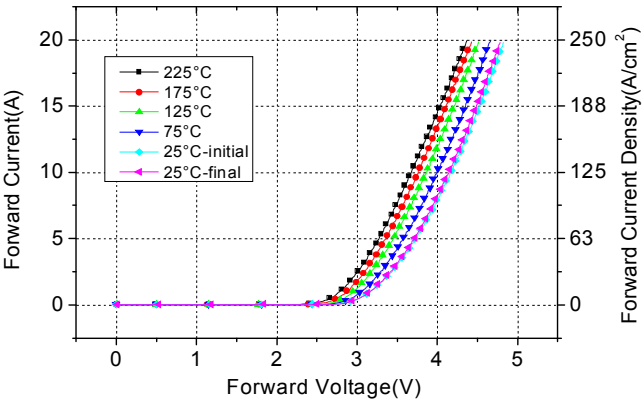
6.5kV diodes design and fabrication have been validated in term of blocking voltage by reverse characterization in a vacuum chamber. The diodes show also a low leakage current at temperature as high as 225°C. The next section presents diodes forward performance.

3.2. Forward characteristics

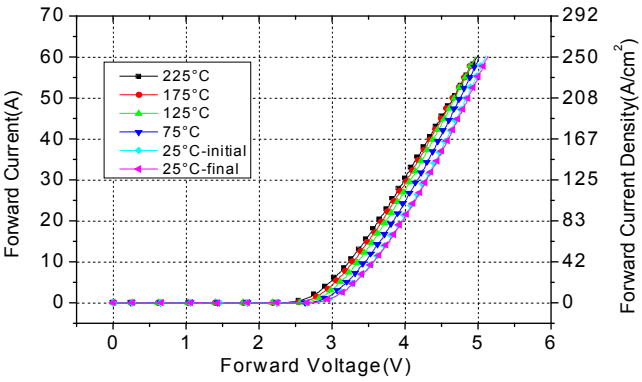
Forward characterizations have been performed on encapsulated diodes. Typical forward characteristics are presented respectively in Fig. 5 (a, b, c) for 2, 8, and 24mm² diode.



(5a)



(5b)



(5c)

Figure 5. Forward characteristics temperature dependence of 2mm² (5a), 8mm² (5b) and 24mm² (5c) diode

Diodes forward performance has been characterized up to a current density of 250A.cm^{-2} corresponding to 60A for the 24mm². To limit the device auto-heating, these characteristics have been obtained in pulse mode with a pulse width of 200µs. At 250A.cm^{-2}, the voltage drop is 4.5V for the 2 and 8mm² diodes and 5V for the 24mm² diodes. These values of voltage drop are high with respect to state of the art [4]. This can be due to the high ohmic contact resistance because the ohmic contact of fabricated diodes as measured on TLM test structures is not very good and a high value of contact resistance of about 25mΩ.cm^{-2} is

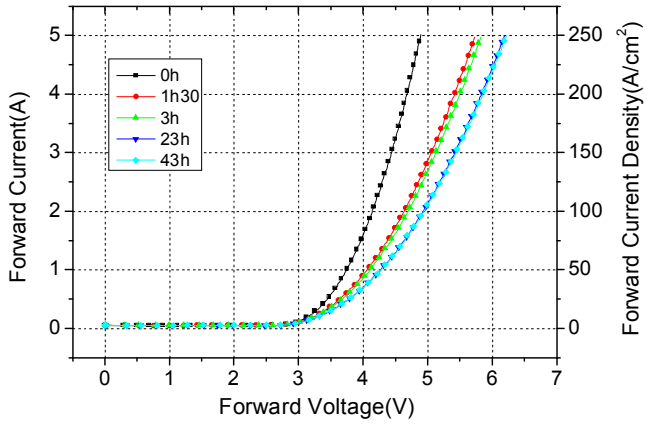
extracted. The increase in voltage drop for the largest diodes is probably due to an insufficient number of bonded wires (6 wires of 125µm diameter for 24mm^2 diodes) leading to a bad current spreading. We can also see that the on-state voltage drop decreases with increasing temperature. The decrease of voltage drop is explained by the increase of carrier lifetime with temperature. This decrease of on-state voltage could be seen as a handicap because thermal excess can occur. However the change in voltage drop remains low, less than 0.5V in the tested temperature range. It is noted that SiC bipolar devices have a threshold voltage of about 3V thus these devices require a case with good thermal conductivity. Targeting a current density of 80A.cm^{-2}, a case with a thermal conductivity of 300W.cm^{-2} and a high voltage capability must be used.

The forward and reverse electrical characteristics measured at 25°C after thermal stress do not show any performance degradation so these diodes are stable with temperature. The next section presents and discusses the influence of electrical stress on the diodes performance.

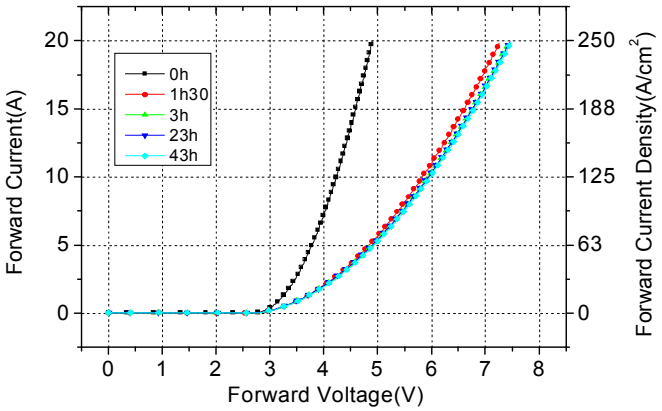
4. ELECTRICAL STRESS

4.1. Evolutions of diode characteristics

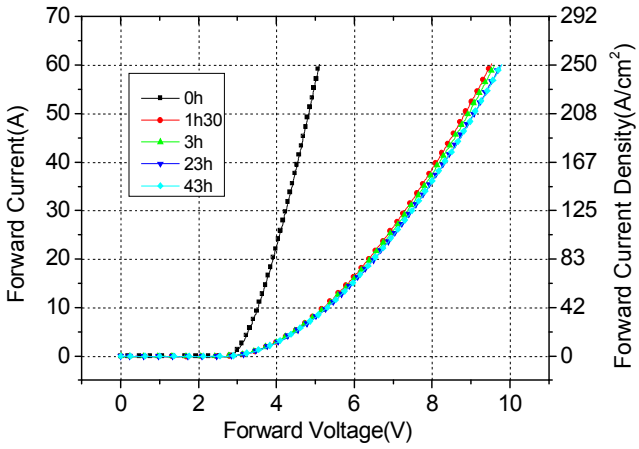
The electrical stress has been performed on the all three diode types. Stress condition is defined by a continued bias forward voltage to maintain a constant current density of 100A.cm^{-2}. For a thermal equilibrium, the diodes are mounted on a radiator with cooling fan. Diodes forward and reverse measurements have been taken at 25°C after 1h30, 3h, 23h and 43h stress time. It is noted that no sub threshold forward nor reverse characteristic change are observed. By contrast, high current forward characteristics are damaged. Typical forward characteristics evolutions are shown respectively in Fig. 6 (a, b, c) for 2, 8, and 24mm^2 diode. An important forward voltage drift has been observed for the three diodes. The most important degradation occurs in the first 1h30 stress time. After 23h stress time, the voltage drift stabilizes and then reaches the saturation. We can also see that the larger diode active area is, the more important degradation is. These observations are interpreted in the next section.



(6a)



(6b)



(6c)

Figure 6. Forward characteristics evolutions of 2mm^2 (6a), 8mm^2 (6b) and 24mm^2 (6c) diode

4.2. Diodes forward degradation interpretation

It is known that the presence of basal plane dislocation (BPDs) can generate stacking faults (SFs). These SFs act as recombination centers which reduce the carrier lifetime. Electron-hole pair recombination at the BPDs in forward mode conduction leads to the propagation of SFs thus increases the voltage drop of bipolar devices [5, 6]. So our diodes forward performance degradation can be explained by the presence of BPDs and the expansion of SFs within the diodes active area. As the quantity of BPDs within a device active area is finite, a finite quantity of SFs can thus generate. Furthermore, there is a finite space for the SFs to expand through (drift layer thickness), the total possible affected area is also finite. Thus, the voltage drift saturation observed above is interpreted by the expansion of every SFs through the drift layer and the possibility of a larger BPDs density within the large active area diode explains the more important degradation for these diodes. In the next section of the paper, the electronic energy level of these SFs determined by admittance spectroscopy technique is presented and we also measure the reduction of carrier lifetime induced by these SFs using open-circuit voltage decay technique (OCVD).

Admittance spectroscopy technique allows detecting defects and extracting their activation energy. This technique has been used to characterize 4H-SiC junction barrier Schottky diodes in a previous paper [7]. It consists in applying a small sinusoidal voltage to the structure and to measure the subsequent capacitance Cp and conductance Gp of the space charge region of the diode. In the presence of a defect centre, the emission and capture kinetic processes of free carriers by the defect centre modify the capacitance and conductance of the structure. By varying frequency and temperature, it is possible to determine the activation energy and the capture cross section of the defect. Indeed, the presence of a defect involves the presence of a peak of conductance as a function of temperature. The temperature T of this maximum is varying with frequency, and for this maximum, the frequency is equal to the thermal emission rate of the defect. The scanned region is situated near the cross of the Fermi level with the defect level. Thus, in an ideal n-type Schottky diode, it is possible to detect only electron traps. But in the presence of a pn junction, it is possible to detect electron trap in the n-type region and hole trap in the p-type region.

In practice, temperature ramps are imposed to the sample, while measuring Cp and Gp for 20 different frequencies. Measurements are performed in a liquid nitrogen cryostat, with an impedance analyser HP4194A for frequencies varying between 300Hz and 20kHz. The frequency range is adjusted in order to detect presented defects in the structure. An Arrhenius plot of ln(ω/T2) vs. 1/T allows to determine the energy level of the defect.

Fig. 7 shows conductance spectra obtained on a stressed diode. These conductance peaks is induced by the presence of a defect and its signature is plotted in Fig. 8. For the virgin diode, no peak of conductance is detected in this temperature range. So these conductance spectra can be attributed to an electrical signature of SFs. It corresponds to an electron trap situated at 0.18eV under conduction band.

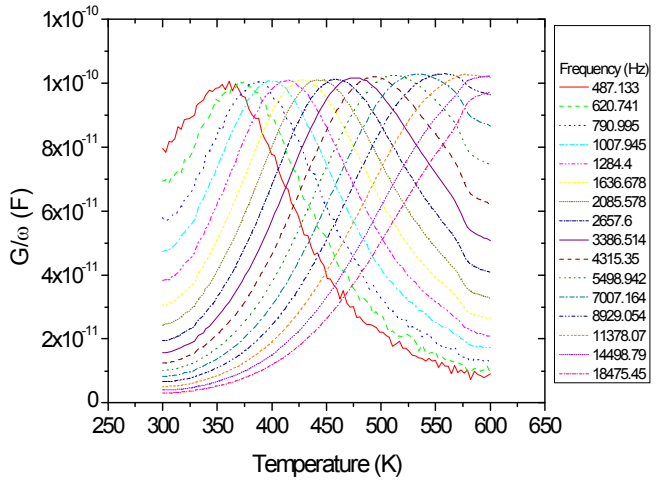


Figure 7. Normalized conductance vs. temperature for 16 different frequencies obtained on a stressed diode

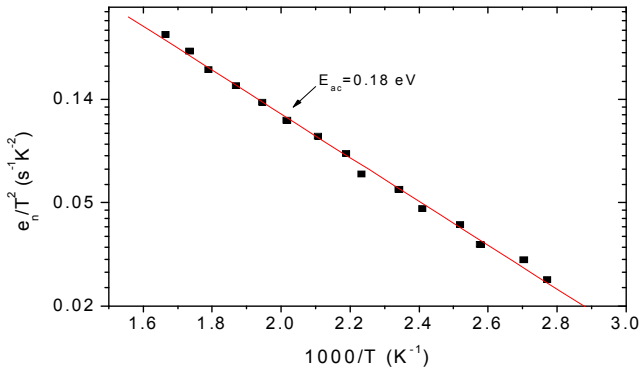


Figure 8. Arrhenius plot of the defect signature

The OCVD technique has been performed to evaluate the ambipolar lifetime of diode before and after electrical stress. This technique consists to integrate the diode into a chopper circuit with a high speed switching device (Si-MOSFET) and to measure the voltage transient across the diode following the abrupt switching-off of the current from a high current injection level [8]. The subsequent voltage decrease is related to the ambipolar lifetime by the following equation [9]:

$$\tau = \tau_n + \tau_p = \frac{2kT}{q}\left(\frac{dV}{dt}\right)^{-1} \quad (1)$$

where (dV/dt) is the slope of the linear part in the voltage decay curve, q is the elementary charge, T is absolute temperature, and k is the Boltzmann constant.

Fig. 9 presents the OCVD voltage transient measured on a diode before and after stress at room temperature using a forward current density of 100A.cm^{-2}. As seen in the figure, the linear part slope of the stressed diode is two times higher than the virgin diode. It means that the ambipolar lifetime is reduced two times for the stressed diode. The ambipolar lifetime is found to be respectively 2470ns and 1400ns using Eq. 1 for the diode before and after stress. Simulated results using Sentaurus with ambipolar lifetime of 2600ns and 1600ns have been also presented in Fig. 9. Electrons and holes lifetimes are supposed to be equal in the simulations. A good agreement between experimental and simulated curves is observed.

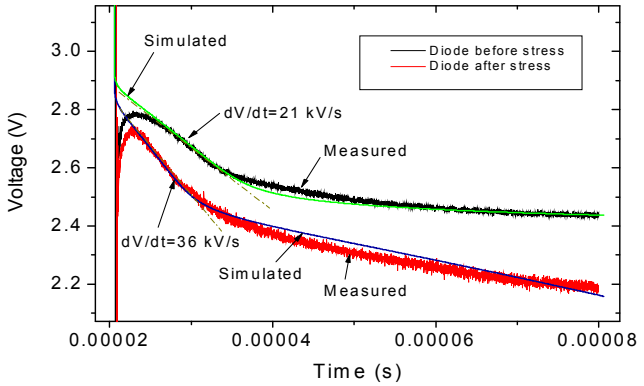


Figure 9. Measured and simulated curves OCVD voltage transient characteristics of a diode before and after electrical stress

Two electrical techniques have been performed justifying the presence of SFs and their influence on the carrier lifetime reduction. This reduction results in a forward voltage drift. On the other hand, as the diodes ohmic contact is not stabilized, this can also contribute partly to the important forward voltage drift of stressed diode. Because, under the high current density stress, the temperature can be high then damaging the contact properties.

5. CONCLUSION

6.5kV 4H-SiC diodes have been designed and fabricated with three different active areas of 2, 8, and 24mm^2. Blocking voltage of 6.5kV has been achieved for the three diodes types. These diodes present a low leakage current and stable operation with temperature up to 225°C and 3kV. Electrical stress at a current density as high as 100A.cm^{-2} has been also performed on these diodes. An important forward voltage drift has been observed. This is due to the generation and expansion of SFs in the diodes drift layer under forward conduction. The SFs presence and their influence have been demonstrated using two electrical methods: OCVD and admittance spectroscopy. OCVD measurements determined a carrier lifetime reduction of up to two times. Admittance spectroscopy measurements revealed an electronic energy level of 0.18eV under conduction band.

REFERENCES

[1]. D. Tournier, P. Brosselard, C. Raynaud, M. Lazar, H. Morel, and D. Planson, 2011. *Wide Band Gap Semiconductors Benefits for High Power, High Voltage and High Temperature Applications*. Advanced Materials Research, 324, 46-51.

[2]. Sentaurus, TCAD simulation tool by Synopsys Inc.

[3]. D-M. Nguyen, C. Raynaud, N. Dheilly, M. Lazar, D. Tournier, P. Brosselard and D. Planson, 2011. *Experimental determination of impact ionization coefficients in 4H-SiC*. Diamond & Related Materials, 20, 395-397.

[4]. D. Peters, W. Bartsch, B. Thomas, and R. Sommer, 2010. *6.5kV SiC PiN Diodes with Improved Forward Characteristics*. Mater. Sci. Forum, 645-648, 901-904.

[5]. J. P. Bergman, H. Lendemann, P. A. Nilsson, U. Lindefelt, and P. Skytt, 2001. *Crystal Defects as Source of Anomalous Forward Voltage Increase of 4H-SiC Diodes*. Mater. Sci. Forum, 353-356, 299-302.

[6]. M. Skowronski and S. Ha, 2006. *Degradation of hexagonal silicon-carbide-based bipolar devices*. J. Appl. Phys. , 99-01101, 01-23.

[7]. C. Raynaud, D-M. Nguyen, P. Brosselard, A. Perez-Tomas, D. Planson, and M. Milan, 2009. *Characterization of 4H-SiC Junction Barrier Schottky Diodes by Admittance vs Temperature Analyses*. Mater. Sci. Forum, 615-617, 671-674.

[8]. N. Dheilly, D. Planson, P. Brosselard, J. Hassan, P. Bevilacqua, D. Tournier, J. Montserrat, C. Raynaud, H. Morel, 2009. *Measurement of Carrier Lifetime Temperature Dependence in 3.3kV 4H-SiC PiN Diodes using OCVD Technique*. Mater. Sci. Forum, 615-617, 703-706.

[9]. S. Bellone, H. C. Neitzert, and G. D. Licciardo, 2004. *An Analog Circuit for Accurate OCVD Measurements*. Solid-State Electronic, 48, 1127-1131.

THÔNG TIN TÁC GIẢ

Nguyễn Duy Minh[1], Nguyễn Mạnh Quân[2]

[1]Khoa Kỹ thuật điện, Trường Đại học Điện lực

[1]Khoa Điện, Trường Đại học Công nghiệp Hà Nội