

# MULTI-WAVELENGTH ALL-OPTICAL PACKET SWITCHING NODE USING MODIFIED PULSE POSITION MODULATION HEADER PROCESSING

NÚT CHUYỂN MẠCH GÓI TOÀN QUANG ĐA BƯỚC SÓNG  
SỬ DỤNG XỬ LÝ MÀO ĐẦU ĐIỀU CHẾ VỊ TRÍ XUNG SỬA ĐỔI

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## ABSTRACT

Optical packet switching (OPS) technologies are among the most promising solutions for Next Generation Network architectures. However, in OPS networks, the header processing time is a main factor that limits network performance. In this paper, we propose an all-optical packet switching node architecture using modified pulse position modulation (MPPM) header processing scheme for packet routing in all-optical highspeed multi-wavelength packet switching network, which is able to improve the network performance. The proposed node is investigated and simulated to show that MPPM-based header processing helps to reduce the header processing time, increase the optical signal-to-noise ratio (OSNR) in comparison with conventional PPM-based header processing.

**Keywords:** Optical packet switching (OPS), synchronous OPS switching with fixed-sized packets, MPPM-based optical packet header processing.

## TÓM TẮT

Công nghệ chuyển mạch gói toàn quang (OPS) là một trong những giải pháp hứa hẹn nhất cho các kiến trúc mạng thế hệ tiếp theo. Tuy nhiên, trong các mạng OPS thời gian xử lý mào đầu là nhân tố chính làm hạn chế hiệu năng mạng. Trong bài báo này, tác giả đề xuất một kiến trúc nút chuyển mạch gói toàn quang sử dụng sơ đồ xử lý mào đầu điều chế vị trí xung sửa đổi (MPPM) cho định tuyến gói cho mạng chuyển mạch gói quang đa bước sóng tốc độ cao, có khả năng cải thiện được hiệu năng mạng. Nút được xuất được khảo sát và mô phỏng để chỉ ra là xử lý mào đầu dựa trên MPPM giúp giảm thời gian xử lý mào đầu và tăng OSNR so với xử lý mào đầu dựa trên PPM thông thường.

**Từ khóa:** Chuyển mạch gói quang (OPS), Chuyển mạch OPS đồng bộ với các gói kích thước cố định, xử lý mào đầu gói quang dựa trên MPPM.

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## 1. INTRODUCTION

Telecommunication networks are experiencing a dramatic increase in demand for capacity. The wide range

of future services will require networks to handle diverse forms of traffic. Optical packet switching (OPS) has attracted considerable research interest because of its potential to achieve higher capacity and increased flexibility. Migrating switching functionality from electronics to optics can resolve the electrical-optical-electrical conversion bottleneck in optical networks. Optical packet switching also offers a finer band-width granularity than circuit switching, enabling more efficient bandwidth sharing among different applications [1]. In an OPS network, data is transported from one node to another in the form of packets [2].

The generic network architecture is shown in Fig. 1. A number of electronic client networks are connected to an edge node (EN). At the edge node, arriving electronic packets are aggregated and encapsulated in optical packets for more efficient utilization of the core network. Then the packets are injected into the optical core nodes (CNs). The packets hop between core nodes with the payload remaining optical to finally arrive at the destination edge node. At the destination edge node the payload is converted back to the electronic domain and delivered to the destination electronic client network [3].

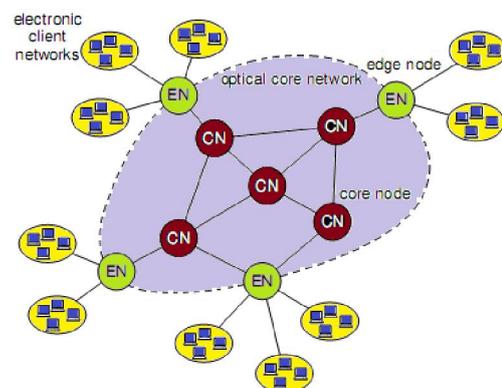


Fig. 1. General architecture of an optical packet-switched network.

In general, packet-based optical networks can be divided into two categories: un-slotted asynchronous

networks with fixed-sized or variable-sized packets and time-slotted synchronous networks with fixed-length packets or variable-sized packets [4]. In a synchronous network, all the input packets have or have not the same size and are aligned in phase before entering the switching matrix. In an asynchronous network, the packets may or may not have the same size and they arrive and enter the switch without being aligned. Therefore, the packet-by-packet switch action can occur at any point in time [1]. In this work, we focus on synchronous switching with fixed-sized packets.

In conventional OPS networks, the packet headers have to be converted to electronic form and processed electronically [5]. As the data channel bandwidth increases dramatically, the electronic header processing is likely to become the performance bottleneck. Therefore, it is imperative to reduce the header processing time in order to improve the network performance.

An effective method for reducing header processing time is the use of pulse position modulation (PPM)-based header processing, in which the packet header processing is carried out in the optical domain. In recent years, many works has been devoted to the study of header processing for optical packet switching networks. However, only a few works have been done for PPM-based header processing [6-9].

In this paper, we propose a modified PPM-based header processing technique, which has an ability of reducing processing time (i.e., reducing routing table entries and correlation processing time) thus help to improve the network performance.

The paper is organized as follows. Firstly, Section 1 is the introduction. Then, the architecture of the proposed node as well the principle operations of node is described in Section 2. The numerical and simulation results are also investigated and discussed in Section 3. Finally, Section 4 will conclude the paper.

**2. PROPOSED MULTI-WAVELENGTH ALL-OPTICAL PACKET SWITCHING NODE ARCHITECTURE**

**2.1. Modified PPM-based header processing**

A typical packet is composed of the clock, address header and payload bits as shown in Fig. 2.

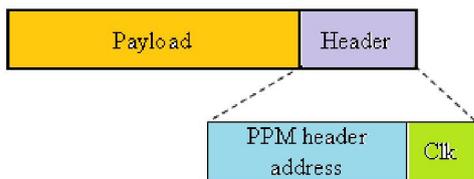


Fig. 2. An optical packet with a PPM based header structure

The clock information is used for synchronization within the node. The data of  $N$ -bit binary codeword contains the destination address, where each bit "1" is encoded as an optical pulse. In PPM a  $N$ -bit binary codeword is mapped into a single frame of  $2^N$ -slot length with a short pulse

located at the  $m_A^{th}$  slot, the position of which corresponds to the decimal value of the  $N$ -bit binary packet header address. A  $N$ -bit address of  $\{a_{N-1} a_{N-2} \dots a_2 a_1 a_0\}$  will have the decimal metric  $m_A$  is computed by:

$$m_A = a_{N-1}2^{N-1} + a_{N-2}2^{N-2} + \dots + a_22^2 + a_12^1 + a_02^0 \quad (1)$$

Thus, in PPM, the information is the conveyed by the position ( $m_A$ ) of a single pulse within a fixed frame.

In contrast to the conventional PPM header address which is binary, we have adopted a control binary field (C bits) and  $N-C$  bits PPM mapping field in MPPM header address. Here the control binary field corresponds to  $C$  ( $2^C \geq M$ ), where  $M$  is the number of node outputs), which controls to select MPPM routing sub-tables (MPPRSTs) and the remaining bits represent a PPM frame of the length  $2^{N-C}$  with a pulse located in the position corresponding to the decimal value of  $\{a_{N-C} \dots a_2 a_1 a_0\}$ . Our preliminary work on the modified pulse position modulation (MPPM) header processing scheme was presented in [10].

**2.2. PPM routing sub-table**

Assuming that the packet header has  $N$  bits address  $\{a_{N-1} a_{N-2} \dots a_2 a_1 a_0\}$ , where  $a_{N-1}$  is the most significant bit (MSB), the conventional routing table (RT) will have a maximum of  $2^N$  entries. In the worst case scenario i.e. checking all entries, the node will perform  $2^N$   $N$ -bitwise correlations.

In the standard pulse position modulation, routing table (PPRT) has  $M$  entries  $E_i$  ( $i = 1, 2, \dots, M$ ) of length  $2^N$  slots with duration  $T_s$ . Here  $T_s = NT_b/2^N$ . The locations of the short pulses in each entry correspond to the decimal values of conventional binary address patterns in  $i^{th}$  group. In MPPM-based header processing scheme, routing table could be made by splitting into  $M$  sub-tables, which has entries. The PPRST entry length could be reduced  $i^{th}$  sub-table. In PPRSTs, entry length could be reduced to  $2^{N-C} \times T_s$ .

**2.3. Multi-wavelength all-optical packet switching node architecture using MPPM-based header**

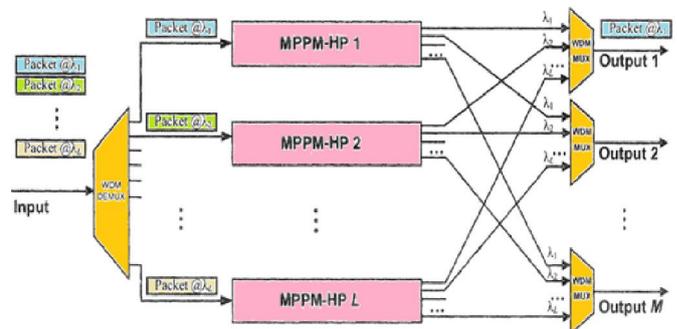


Fig. 3. Block diagram of the proposed 1xM multi-wavelength all-optical packet switching node based on PPM-HPs

Figure 3 shows schematic block diagram a typical OPS node with the proposed header processing units. The node composed of a  $1 \times L$  WDM demultiplexer,  $L$  MPPM-HP modules, and  $M L \times 1$  WDM multiplexers, where  $L$  is the number of wavelength. In this figure, at the node input,

multi-wavelength ( $\lambda_1, \lambda_2, \dots, \lambda_L$ ) packets are passed through a demultiplexer before being fed to a bank of MPPM-HP modules. Each MPPM-HP module  $l^{th}$  ( $1 \leq l \leq L$ ) is assigned to process the packets at a given wavelength  $\lambda_l$ . Packets with the MPPM format header address at specific wavelength are processed at the MPPM-HP modules before being broadcasted to all  $L \times 1$  WDM multiplexers. In contrast to existing schemes this architecture uses fewer number of laser sources because there is no need for wavelength conversion modules.

The MPPM-HP module with M-output ports comprises of clock extraction module (CEM), MPPM header extraction module (MPPM-HEM), a MPPM routing table (MPPM-RT) generator, a bank of all-optical AND gates, a number of SMZ based all-optical switches (OS) and an OS control module (OSC), see Fig. 4. The incoming packet  $P_{in}(t)$  at the given wavelength  $\lambda_l$  is split and applied to CEM, MPPM-HEM, and OS with delays of 0,  $T_{CEM}$  (required time for clock extraction) and  $T_{MPPM-HP}$  (total required time for MPPM header processing), respectively. The extracted clock signal  $Clk(t)$  and its delay version are applied to the MPPM-HEM and MPPRT modules with the delays of  $T_{ACM}$  and  $T_{MPPRT}$ , respectively, for extracting and converting the address bits to MPPM format and for generating MPPRT, respectively. The CEM, MPPM-HEM and MPPRT generator modules configurations was presented in [11]. At the input of MPPM-ACM, the signal  $x(t)$  is  $\alpha \cdot Clk(t + T_{ACM})$  where  $\alpha$  is the splitting factor.  $N$ -bit packet header address extracted from the packet by the SPC and  $(N-C)$ -bit converted to the MPPM format at the output is defined by:

$$x_{MPPM}(t) = x \left( t + \sum_{i=0}^{N-C-1} a_i \cdot 2^i \cdot T_s \right), \quad a_i \in \{0, 1\} \quad (2)$$

Where  $x(t)$  and  $x_{MPPM}(t)$  are the input and output signals at the MPPM address conversion module (MPPM-ACM), respectively. The bit  $a_i$  (0 or 1) is the  $i^{th}$  bit in  $(N-C)$ -bit address,  $T_s$  is a defined MPPM-slot duration.

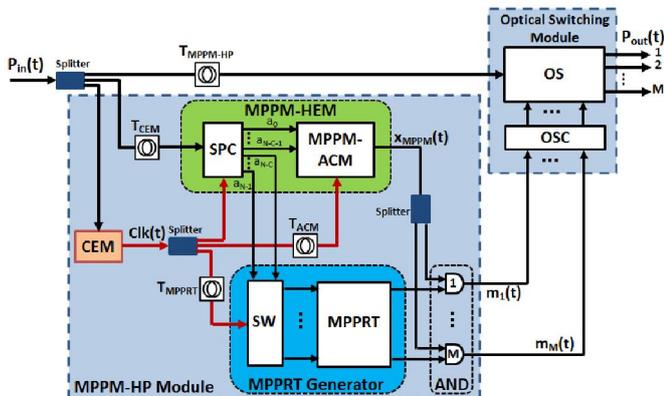


Fig. 4. Block diagram of the proposed  $1 \times M$  multi-wavelength all-optical packet switching node based on PPM-HPs

A fraction of the extracted single clock pulse  $Clk(t)$  will go to MPPRT generator to check the status of  $a_{N-1}, a_{N-2}, \dots$  and  $a_{N-C}$  singly for controlling SW. The input pulses will emerge at one of outputs of a SW as a single pulse  $e_i(t)$  to

select sub-routing table and to generate corresponding  $E_i(t)$  ( $i = 1, 2, \dots, M$ ). Packet header address identification is carried out by correlating the extrated MPPM-header address with the MPPRT entries using only one AND gate in the bank of all-optical AND gates. The matching pulse  $m_i(t)$  will be then sent to the OSC module to ensure that the incoming packet  $P_{in}(t)$  delayed by  $T_{MPPM-HP}$  is switched to the correct output port.

2.4. Performance analysis

Header processing time:

Header processing time,  $T_{HP}$  is defined as the period of time from when the packet arrived until the header processors find the control information. In the OPS networks using MPPM-based header processing, the processing time includes the required time for clock extraction,  $T_{CE}$  and the required time for header recognition,  $T_{HR}$ . Header recognition includes the MPPM-address conversion (in MPPM conversion module) and correlation times between MPPM header address and a MPPRT entry (to the only one AND gate). Since both tasks could be carried out simultaneously, the header recognition time due to MPPM-based header processing,  $T_{HR}$  is determined by:

$$T_{HR} = 2^{N-C} \cdot T_s + T_{AND} \quad (3)$$

Thus, the analytic expression for header processing,  $T_{HP}$ , can be written in the form:

$$T_{HP} = T_{CE} + 2^{N-C} \cdot T_s + T_{AND} \quad (4)$$

Where  $T_{AND}$  is the clock extraction time and  $N$  is the header address bits and  $T_s$  is the slot duration.

3. NUMERICAL AND SIMULATION RESULTS

In this section, we compare the OPS networks using our proposed header processing scheme to other OPS using conventional PPM-based header processing scheme. The comparison is based on several parameters including header processing time,  $T_{HP}$  and optical signal-to-noise ratio (OSNR).

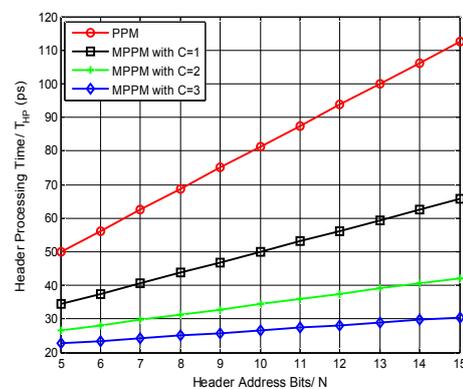


Fig. 5. Header processing time versus the header address bits when  $C=1, C=2$  or  $C=3$ ;  $T_b = 6.25ps$  ( $R_d = 160Gb/s$ );  $T_{CE} = 12.5ps$ ;  $T_{AND} = 6.25ps$

Now, we analyze the results concerning the header processing time based on Eq.(4). These results are shown in

Fig. 5, where header processing time versus the header address bits is investigated. We can see that the MPPM-based header processing time is in the scale of picosecond, which is very short compared with conventional electronic header processing (approximately  $10\mu s$  [12]). Also, in our proposal, the header processing time is reduced four times with  $C = 3$  in comparison with conventional PPM-based header processing time.

The operation principle and OSNR performance of the node are demonstrated by numerical simulation using the OptiSystem simulation software. The node simulation model is based on Figs. 3, and 4. A block diagram of the PPM-HP and MPPM-HP modules is shown in Fig. 6a and Fig. 6b, respectively. The main simulation parameters used are given in Tables 1 and 2. Each packet contains one clock bit,  $N = 5$  address bits,  $C = 2$  control bits and a long payload. Packets at wavelength  $\lambda_1$  and  $\lambda_2$  are applied to the node (eight packets are transmitted in each wavelength) having high input OSNR of  $\sim 32$  dB. Packet header addresses (in decimal values) are listed in Table 3 where the number  $m$  in brackets indicates that packet will be switched to the  $m_{th}$  ( $1 \leq m \leq M$ ) node output.

Table 1. Simulation system parameters

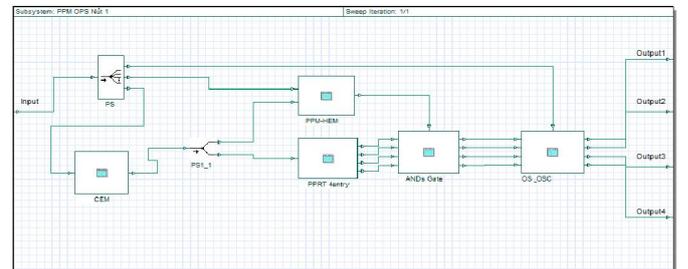
System Parameters	Values
Data packet bit rate- $1/T_b$	160 Gb/s
Packet payload length	64 Byte
Data packet guard time	1 ns
Wavelength 1- $\lambda_1$	1552.52 nm
Wavelength 2- $\lambda_2$	1544.52 nm
Number of node outputs	4
Data pulse width-FWHM	2 ps
Bit duration- $T_b$	6.25 ps
Average transmitted packet pulse peak power- $P_{in}$	2 mW
Optical bandwidth	500 GHz
Splitting factor - $\alpha$	0.25
Number of control pulse	256
Average control pulse power	10 mW

Table 2. SOA parameters

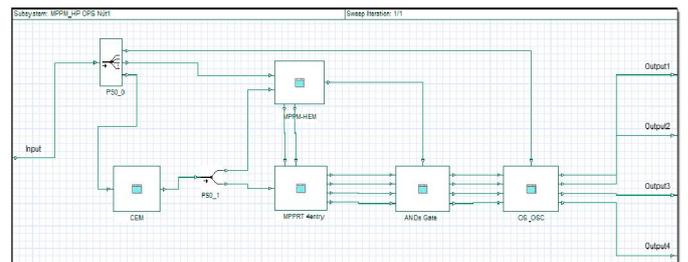
SOA Parameters	Values
SOA length- $L_{SOA}$	$500 \cdot 10^{-6}$ m
SOA width- $W_{SOA}$	$3 \cdot 10^{-6}$ m
SOA height- $H_{SOA}$	$80 \cdot 10^{-6}$ m
Optical confinement factor	0.2
Internal loss	$40 \cdot 10^{-2} m^{-1}$
Differential gain	$2,8 \cdot 10^{-20} m^2$
Carrier density transparency	$1,4 \cdot 10^{24} m^{-3}$
Enhancement factor	4
Recombination coefficient A	$1,43 \cdot 10^8 s^{-1}$
Recombination coefficient B	$1 \cdot 10^{-6} m^3 s^{-1}$
Recombination coefficient C	$3 \cdot 10^{-41} m^6 s^{-1}$
Initial carrier density	$3 \cdot 10^{24} m^{-3}$
DC bias current	150 mA

Table 3. Addresses of the incoming packets to the node

Wave length	Address of packet 1	Address of packet 2	Address of packet 3	Address of packet 4	Address of packet 5	Address of packet 6	Address of packet 7	Address of packet 8
$\lambda_1$	1 (4)	5 (4)	8 (3)	12 (3)	16 (2)	20 (2)	26 (1)	28 (1)
$\lambda_2$	2 (4)	6 (4)	9 (3)	14 (3)	17 (2)	25 (1)	27 (1)	29 (1)



(a)



(b)

Fig. 6. The diagram of (a) PPM-HP modules and (b) MPPM-HP modules

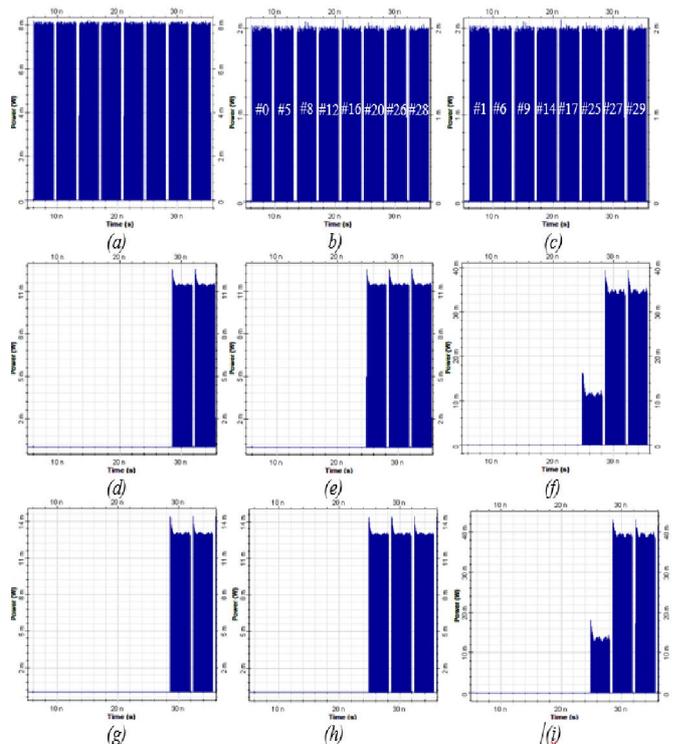


Fig. 7. (a) Packets observed at (a) the input of the node, (b) the input of PPM-HP 1 and MPPM-HP 1, (c) the input of PPM-HP 2 and MPPM-HP 2, (d) the output 1 of PPM-HP1, (e) the output 1 of PPM-HP2, (f) the output 1 of PPM-HP node, (g) the output 1 of MPPM-HP1, (h) the output 1 of MPPM-HP2, (i) the output 1 of PPM-HP node

Figure 7(a) shows the packet waveforms at the node input. Figure 7(b) and (c) shows the packet waveforms at the input of PPM-HPs or MPPM-HPs at two different wavelengths, respectively. The signal waveforms presented in Figs. 7(d) - (f) correspond to the signals with different wavelengths at the input of the multiplexers and the multiplexed signal at the PPM-HP based node output 1, respectively. The signal waveforms presented in Figs. 7(g) - (i) correspond to the signals with different wavelengths at the input of the multiplexers and the multiplexed signal at the MPPM-HP based node output 1, respectively. From the diagrams, the OSNR (between the signal and noise level) is measured more than 25.5 dB and 27 dB correspond to PPM-HP based node and MPPM-HP based node.

#### 4. CONCLUSION

In this paper, we have proposed the multi-wavelength all-optical packet switching node using modified PPM-based header processing for OPS networks. The node architecture, operation principle and performance of the multi-wavelength all-optical packet switching node using MPPM formatted header address were presented. With MPPM-based header processing, the header processing time is reduced significantly hence the network performance is improved. The simulation results show that MPPM-based header processing helps to increase the optical signal-to-noise ratio (OSNR).

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